## Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1-4, 14-17, 21, and 23-26 have been amended. No claims have been cancelled or added. Therefore, claims 1-33 are presented for examination.

## Claim Objections

Claims 1, 14, 21, and 23 stand objected to because the claim limitation "a TOP chain" should be changed to "a TOP-level block (TOP) scan chain". In addition, claims 3, 4, 16, 17, 25, and 26 stand objected to because the claim limitation "TOP chain" should be changed to "TOP scan chain." Applicant submits that claims 1, 3, 4, 14, 16, 17, 21, 23, 25, and 26 have been amended to appear in proper condition for allowance.

## 35 U.S.C. §112 Rejection

Claims 2, 15, and 24 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant submits that the above rejection has been obviated by the amendment to claims 2, 15, and 24.

## 35 U.S.C. §102(e) Rejection

Claims 1-9, 14-29 stand rejected under 35 U.S.C. §102(e) as being anticipated by Nadeau-Dostie et al. (U.S. Pub. No. 2003/0115522). Applicant submits that the present claims are patentable over Nadeau-Dostie.

Nadeau-Dostie discloses a method for designing integrated circuits having a hierarchical architecture to aid quiescent current monitoring of the circuit. The method allows the state of an entire circuit to be set in a repeatable and predictable manner and avoids the need to analyze the entire circuit at once. (See page 1, paragraph 0008). In particular, Nadeau-Dostie discloses configuring scan paths within a circuit to enable efficient quiescent current testing. Internal scan chain segments within a hierarchical block are configured on a scan path by connecting the internal chain segment serial inputs to: (1) a block serial input, (2) the serial output of another segment in the block, or (3) to the serial output of a peripheral segment located in an embedded block one level down in design hierarchy. (See page 4, paragraph 0040). This configuration limits the sources of any peripheral segments in a block to either the block serial input or to the output of another peripheral segment in the block or in an embedded block. (See page 4, paragraph 0041).

Claim1, as amended, of the present application recites:

> A method of providing a single scan chain of a chip, the method comprising:
>
> selecting a TOP-level block (TOP) scan chain of the chip, the chip being divided into a plurality of embedded logic test (ELT) blocks;
>
> identifying scan-in and scan-out ports of periphery flops of the plurality of ELT blocks;
>
> bypassing the scan-in and scan-out ports of the periphery flops of the plurality of ELT blocks;
>
> selecting a single scan chain of all ELT blocks of the chip; and
>
> inserting the single scan chain of all ELT blocks of the chip into the TOP scan chain of the chip.

Applicants submit that there is no disclosure or suggestion in Nadeau-Dostie of identifying scan-in and scan-out ports of periphery flops of ELT blocks and bypassing these scan-in and scan-out ports of the periphery flops of the ELT blocks. Nadeau-Dostie discloses

periphery component inputs as being limited to specific sources, such as from a block input, or from another periphery element. Thus, in Nadeau-Dostie, the peripheral elements must be located at the beginning of a scan path (see page 5, paragraph 0047). Therefore, the Nadeau-Dostie disclosure actually prohibits bypassing the peripheral elements. The Office Action cites multiplexer 82, for selectively connecting the input of peripheral segment 76, as disclosing bypassing periphery flops (see Office Action page 3, point 5). But, the multiplexer disclosed in Nadeau-Dostie operates to select from where the input into the peripheral element is coming from, not to bypass the input into the peripheral element altogether. There is no disclosure or suggestion in Nadeau-Dostie of identifying and bypassing the scan-in and scan-out ports of these peripheral elements.

Furthermore, there is no disclosure or suggestion in Nadeau-Dostie of selecting a single scan chain of all of the ELT blocks of a chip. As disclosed in the specification of the present application at page 6, paragraph [0024] and at Figures 3-5, a single scan chain is the concatentenation of all flops in an ELT block. Nadeau-Dosite, in fact, discloses just the opposite configuration. Nadeau-Dostie creates a configuration with multiple-scan paths within a block, instead of a single scan chain. (See page 4, paragraph 0041). Therefore, claim 1 is patentable over Nadeau-Dostie.

Claims 2-13 depend from claim 1 and include additional limitations. Therefore, claims 2-13 are also patentable over Nadeau-Dostie.

Independent claims 14, 21, and 23 also include similar features as claim 1 (e.g. identifying scan-in and scan-out ports of periphery flops of ELT blocks and bypassing these scan-in and scan-out ports of the periphery flops of the ELT blocks, and selecting a single scan chain of all of the ELT blocks of a chip). As discussed above, Nadeau-Dostie does not

disclose or suggest such features. Therefore, claims 14, 21, and 23 are also patentable over Nadeua-Dostie.

Claims 15-20, 22, and 24-33 depend from independent claims 14, 21, and 23, respectively, and include additional limitations. Therefore, claims 15-20, 22, and 24-33 are also patentable over Nadeau-Dostie.

**35 U.S.C. §103(a) Rejection**

Claims 10, 11, 30 and 31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Nadeau-Dostie et al. (U.S. Pub. No. 2003/0115522), in view of Sato et al. (U.S. Pub. No. 2001/0022743). Applicant submits that the present claims are patentable over Nadeau-Dostie even in view of Sato.

Sato discloses an integrated circuit comprising a storage circuit that can be utilized as a logic circuit. The logic test circuit can be composed on the chip without having to introduce a FPGA (field-programmable gate array). (See Sato at Abstract). Applicant submits that there is no suggestion or teaching in Sato of identifying scan-in and scan-out ports of periphery flops of ELT blocks and bypassing these scan-in and scan-out ports of the periphery flops of the ELT blocks. Likewise, as discussed above, Nadeau-Dostie does not disclose identifying scan-in and scan-out ports of periphery flops of ELT blocks and bypassing these scan-in and scan-out ports of the periphery flops of the ELT blocks. Therefore, any combination of Nadeau-Dostie and Sato would not teach or suggest the claimed invention. Accordingly, claims 10, 11, 30, and 31 are patentable over Nadeau-Dostie in view of Sato.

Claims 12, 13, 32 and 33 stand rejected under 5 U.S.C. §103(a) as being unpatentable over Nadeau-Dostie et al. (U.S. Pub. No. 2003/0115522), in view of Kim et al. (U.S. Patent No. 5,504,756). Applicant submits that the present claims are patentable over Nadeau-Dostie even in Kim.

Kim discloses a method for a multi-frequency, multi-phase scan chain for testing sequential logic circuitry. Scan chains running at different frequency multiples of a base frequency may be concatenated with the output of the last storage element of one scan chain being coupled to the input of the first storage element of the next scan chain. (See Kim at Abstract). Applicant submits that there is no suggestion or teaching in Kim of identifying scan-in and scan-out ports of periphery flops of ELT blocks and bypassing these scan-in and scan-out ports of the periphery flops of the ELT blocks. Likewise, as discussed above, Nadeau-Dostie in view of Sato does not disclose or suggest identifying scan-in and scan-out ports of periphery flops of ELT blocks and bypassing these scan-in and scan-out ports of the periphery flops of the ELT blocks. Therefore, any combination of Nadeau-Dostie, Sat, and Kim would not dislcose or suggest the claimed invention. Accordingly, claims 12, 13, 32, and 33 are patentable over Nadeau-Dostie and Sato, in view of Kim.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

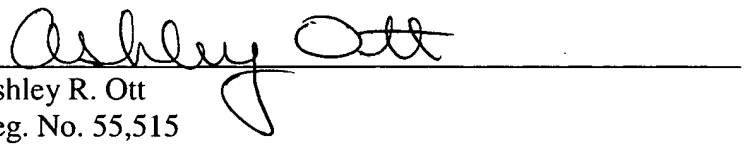
Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: October 14, 2004



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